REMARKS

Claims 1, 14, 18, 21, 24, 29 and 31 have been amended to address the Examiner's claim objection and 112 rejection, clarify the invention, and correct minor informalities. Claim 27 has also been amended to correct a minor informality. No new matter has been entered by any of the foregoing amendments.

Turning to the art rejections, and considering first the rejection of claims 1-3, 18 and 21-31 under 35 USC §102 as anticipated by Loan et al. (U.S. Patent No. 6,136,725), and the rejection of claims 4-6, 11, 13, 14 and 20 under 35 USC §103 as obvious over Loan et al. in view of Stoner et al. (U.S. Patent No. 5,397,428), Loan et al. is 102(e) art, and has a U.S. filing date of April 14, 1998. The subject application is a divisional of U.S. application Serial No. 09/273,627, filed March 23, 1999, and claims priority, via the '627 application, to Japanese Application No. 75195/1998, filed March 24, 1998. A certified copy of Applicant's underlying Japanese priority application is of record in the '627 parent application file. Accompanying this Amendment is a sworn English translation of Applicant's underlying Japanese Application thus perfecting Applicant's priority claim, and removing Loan et al. as citable prior art. With the perfection of Applicant's priority claim, the rejection of claims 1-3, 18 and 21-31 as anticipated by Loan et al. and the rejection of claims 4-6, 11, 13, 14 and 20 as obvious over a combination of Loan et al. and Stoner et al. have been rendered moot.

Turning to the rejection of claims 1-3 under 35 USC §102 as anticipated by Kaloyeros et al. (U.S. Patent No. 6,077,571, cited in parent), the Examiner's rejection is in error. Applicant's claim 1 requires that a d.c. electric potential be supplied to a substrate or a film deposited on a substrate so that the crystal of the deposited phase material is formed in a

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direction of the electric field induced by the d.c. electric potential. This feature of claim 1 is not taught by Kaloyeros et al. Kaloyeros et al. teaches a well known Plasma CVD method using two oppositely charged electrodes placed above and below a semiconductor substrate thereby causing particles to be deposited upon substrate 29. Nowhere does Kaloyeros et al. teach a voltage that is placed across substrate 29, causing a crystalline structure oriented in the direction of the electric potential to be formed. Thus, Kaloyeros et al. cannot achieve or render obvious claim 1, nor claims 2 and 3 which depend therefrom.

The Examiner's double-patenting rejection of claims 1-6, 11, 13, 14, 18, 20, 21, 29 and 31 is noted. Applicant will file a Terminal Disclaimer once Applicant's claims are otherwise indicated to be allowable.

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action are respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account Number 08-1391.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: MAIL STOP AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on November 24, 2004, at Tucson, Arizona.

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ENGLISH TRANSLATION OF JAPANESE

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